

60V N-Channel Power MOSFET

• **General Description**

It combines trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• **Features**

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

• **Application**

- BLDC Motor driver
- DC-DC
- Battery protection

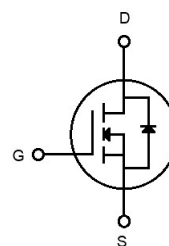
• **Ordering Information:**

Part NO.	ZMA280N06D
Marking	ZM280N06
Packing Information	REEL TAPE
Basic ordering unit (pcs)	2500

• **Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		60	V
Gate-Source Voltage ^①	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^{\circ}\text{C}$	30	A
	I_D	$T_C=75^{\circ}\text{C}$	24	A
	I_D	$T_C=100^{\circ}\text{C}$	21	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^{\circ}\text{C}$;	120	A
Total Power Dissipation	P_D	$T_C=25^{\circ}\text{C}$	60	W
Total Power Dissipation	P_D	$T_A=25^{\circ}\text{C}$	2.4	W
Operating Junction Temperature	T_J		-55 to +175	$^{\circ}\text{C}$
Storage Temperature	T_{STG}		-55 to +175	$^{\circ}\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	25	mJ
		$L=0.5\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	53	mJ
ESD Level (HBM)	CLASS 2			

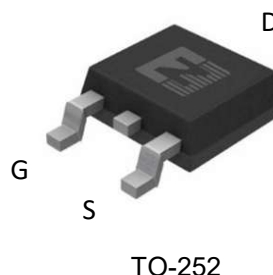
• **Product Summary**



$$V_{DS} = 60\text{V}$$

$$R_{DS(ON)} = 28\text{m}\Omega$$

$$I_D = 30\text{A}$$



•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	2.5	°C/W
Thermal resistance, junction-ambient ^②	R_{thJA}		-	62	°C/W
Soldering temperature	T_{sold}		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.3	1.8	2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=60V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=12A$		28	34	m Ω
		$V_{GS}=4.5V, I_D=8A$		33	40	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_{SD}=10A$		12		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=12A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=25V$	-	1300	-	pF
Output capacitance	C_{oss}		-	53	-	
Reverse transfer capacitance	C_{rss}		-	31	-	
Gate Resistance	R_g	$f=1MHz$	-	1.4		Ω
Total gate charge	Q_g	$V_{DD}=15V, I_D=20A, V_{GS}=10V$	-	17	-	nC
	$Q_g(4.5V)$		-	8	-	
Gate - Source charge	Q_{gs}		-	4.1	-	
Gate - Drain charge	Q_{gd}		-	2.5	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G=3.3\Omega, I_D=20A$	-	9	-	ns
Turn-ON Rise time	t_r		-	32	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	44	-	ns
Turn-Off Fall time	t_f		-	30	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD}=20V, dI_S/dt=100A/\mu s, I_S=20A$	-	50	-	ns
Reverse Recovery Charge	Q_{RR}		-	45	-	nC



Fig.1 Gate-Charge Characteristics

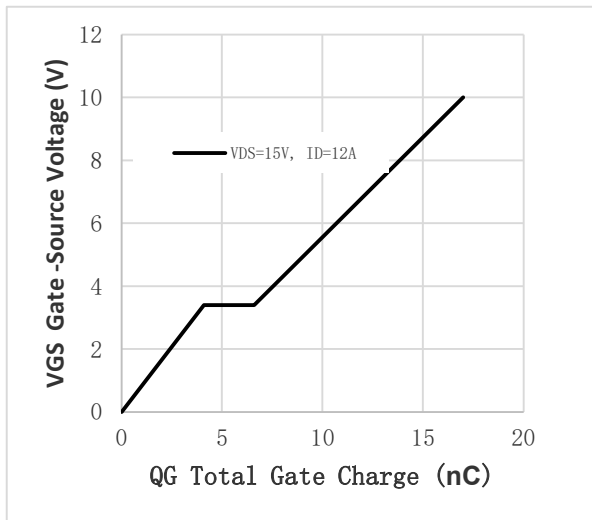


Fig.2 Capacitance Characteristics

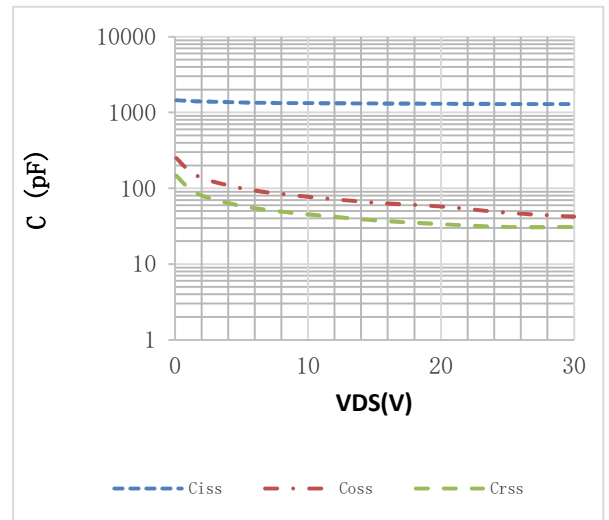


Fig.3 Power Dissipation

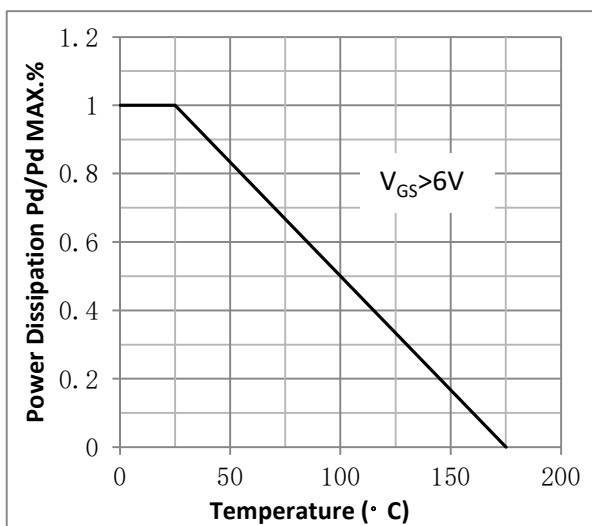


Fig.4 Typical output Characteristics

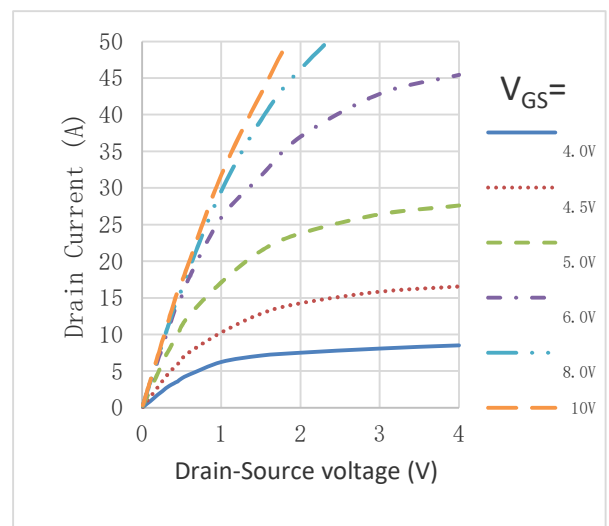


Fig.5 Threshold Voltage V.S Junction Temperature

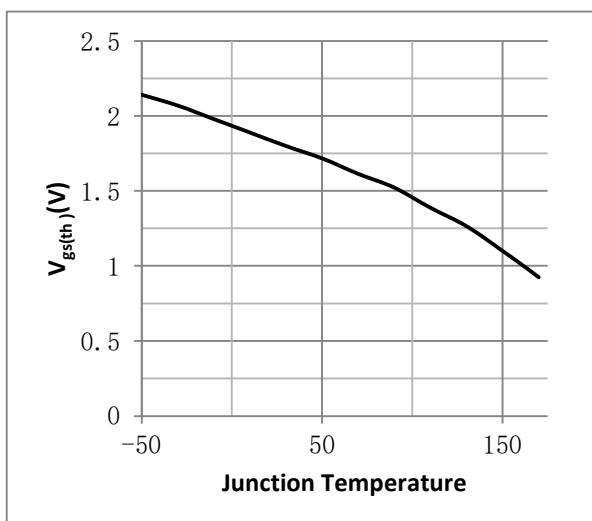


Fig.6 Resistance V.S Drain Current

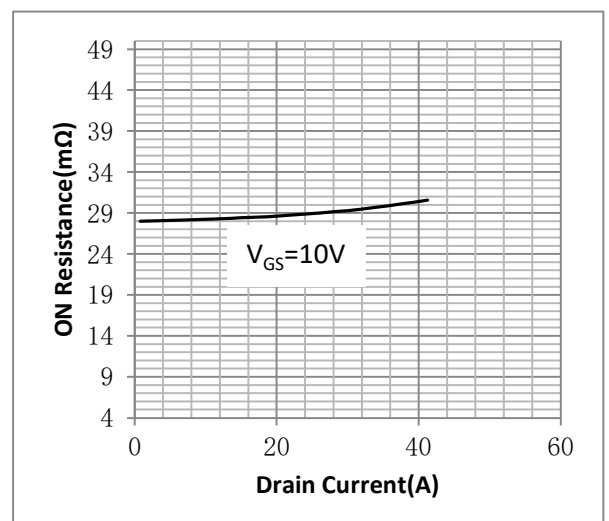


Fig.7 On-Resistance VS Gate Source Voltage

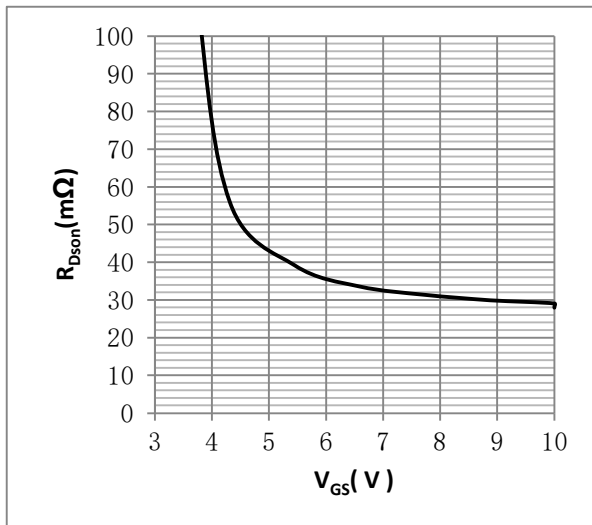


Fig.8 On-Resistance V.S Junction Temperature

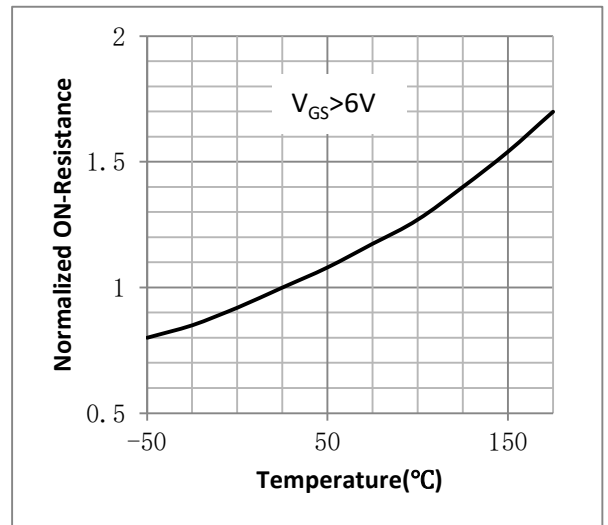


Figure 9. Diode Forward Voltage vs. Current

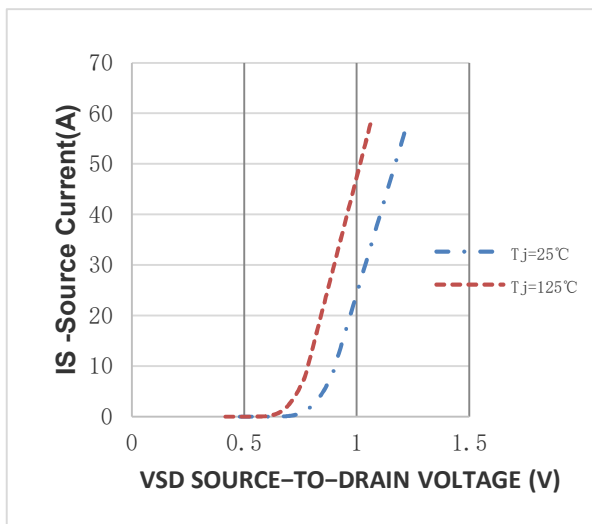


Figure 10. Transfer Characteristics

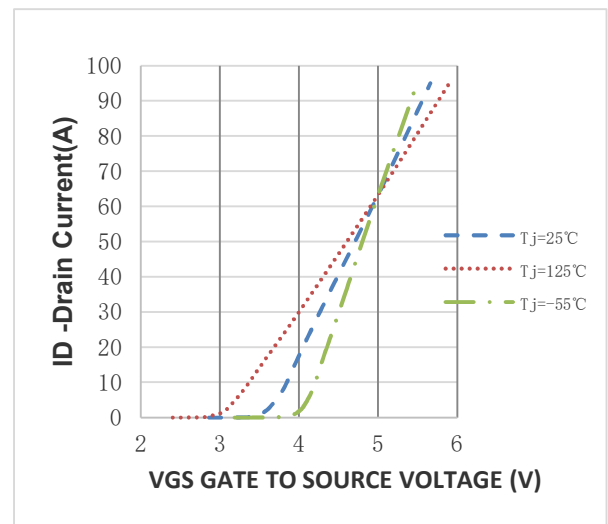


Fig.11 SOA Maximum Safe Operating Area

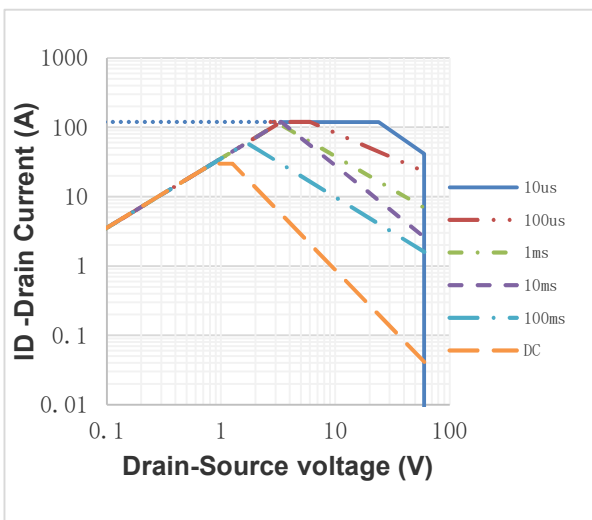
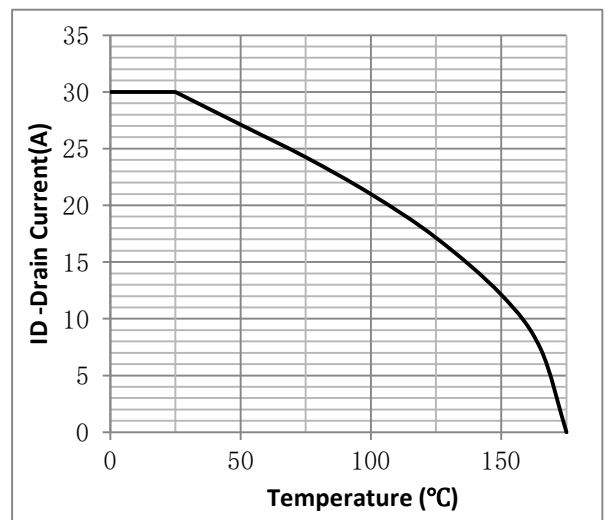
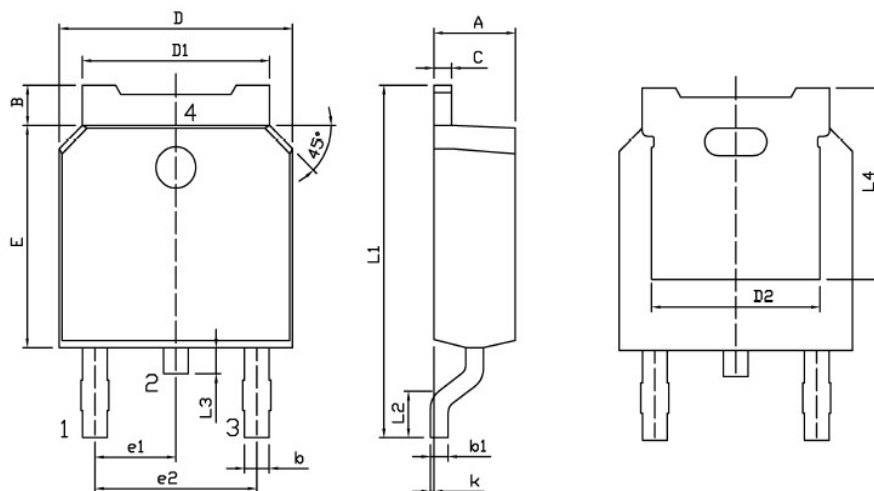


Fig.12 ID vs. Case Temperature^③



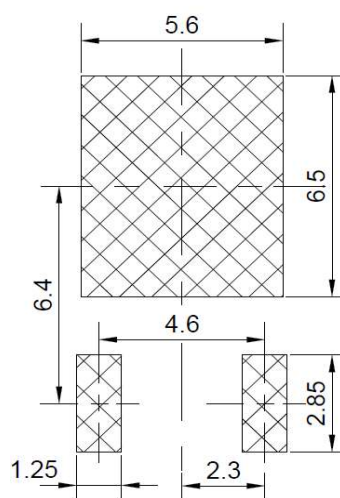
•TO-252 Package Outline

Option L:



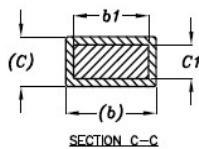
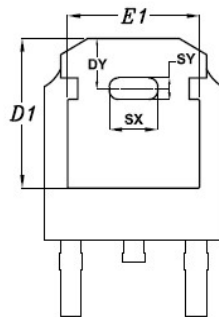
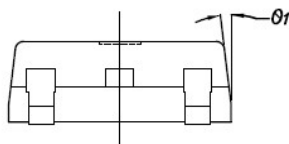
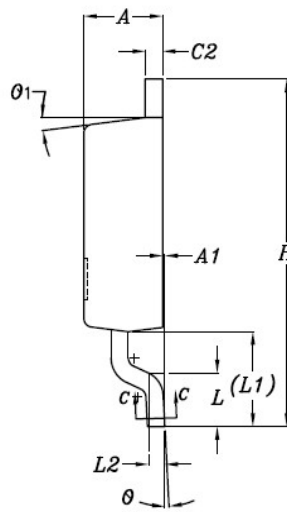
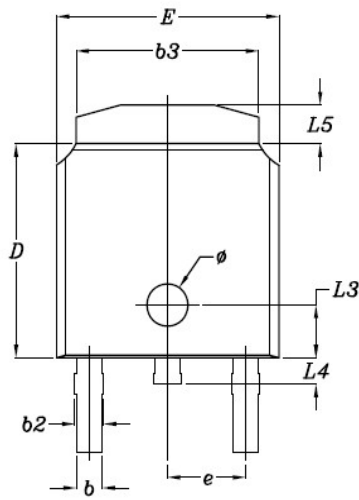
Dimensions In Millimeters					
Symbol	MIN	MAX	Symbol	MIN	MAX
A	2.20	2.40	E	5.95	6.25
B	0.95	1.25	e1	2.24	2.34
b	0.70	0.90	e2	4.43	4.73
b1	0.45	0.55	L1	9.85	10.35
C	0.45	0.55	L2	1.70	2.00
D	6.45	6.75	L3	0.60	0.90
D1	5.10	5.50	L4	5.05	
D2	4.85		k	0.00	0.10

Land Pattern
(Only for Reference)



•TO-252 Package Outline

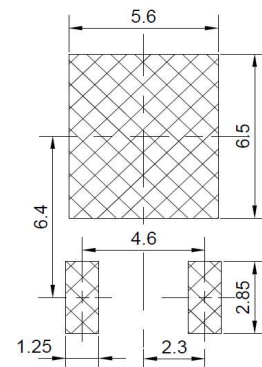
Option Q:



I T E M	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.39	0.086	0.094
A1	—	0.13	—	0.005
b	0.70	0.89	0.028	0.035
b1	0.70	0.86	0.028	0.034
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	5.54	0.205	0.218
E	6.35	6.73	0.250	0.265
E1	4.32	5.27	0.170	0.207
e	2.29 BSC		0.090 BSC	
H	9.40	10.41	0.370	0.410
L	1.40	1.78	0.055	0.070
L1	2.60	2.90	0.102	0.114
L2	0.51 BSC		0.020 BSC	
L3	1.65	1.95	0.065	0.077
L4	0.60	0.90	0.024	0.035
L5	0.89	1.27	0.035	0.050
theta	1°	5°	1°	5°
theta1	7° REF		7° REF	
phi	1.20 REF		0.047 REF	
SX	1.52 REF		0.060 REF	
SY	0.50 REF		0.020 REF	
DY	1.70 REF		0.067 REF	

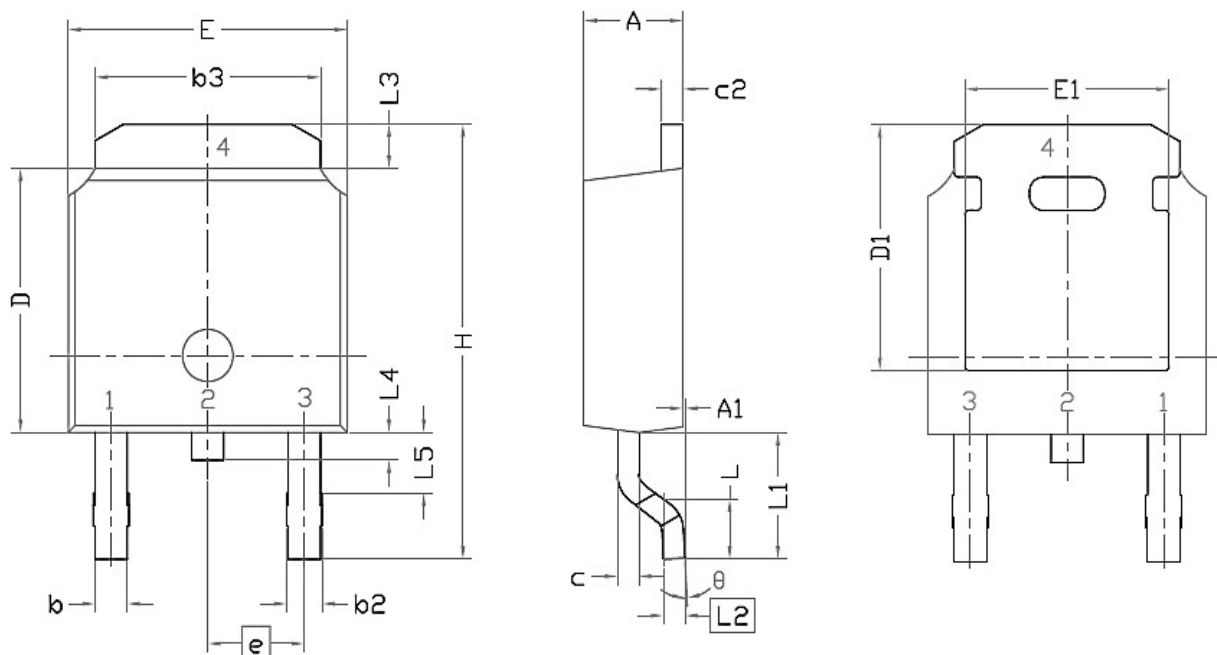


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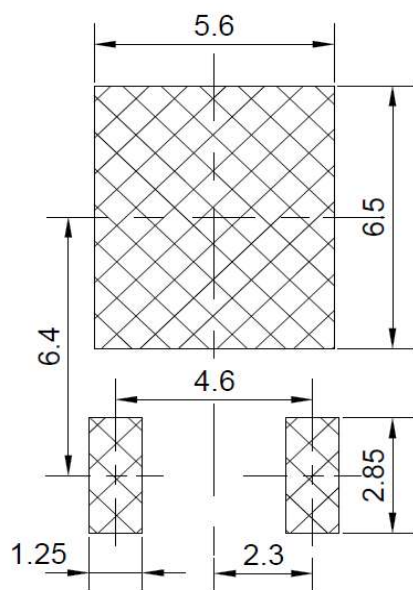


•TO-252 Package Outline

Option M:



Land Pattern
(Only for Reference)



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	--	1.27
L4	0.64	--	1.01
L5	--	--	--
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e	2.286 BSC		
A	2.20	2.30	2.38
A1	0	--	0.127
c	0.46	0.50	0.60
c2	0.46	0.50	0.58
D1	5.21	--	--
E1	4.40	--	--
θ	0°	--	10°

Note:

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=10V$.

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Revision History

Version	Date	Change
A	2021.9.10	
B	2022.9.5	1.Dynamic characteristics 2.Add Reach,HF figure,3.ID modify
C	2025.11.14	Update POD